

K.L.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,578	08/06/2001	Hiromi Nanba	107346-00017	9647

7590

03/27/2002

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
Suite 600
1050 Connecticut Avenue
Washington, DC 20036-5339

EXAMINER

NGUYEN, MINH T

ART UNIT	PAPER NUMBER
----------	--------------

2816

DATE MAILED: 03/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/921,578

Applicant(s)

NANBA ET AL.

Examiner

Minh Nguyen

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 August 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1-6 are objected to because of the following informalities:

In claim 1, line 12, --at-- should be inserted after "replica circuit".

In claim 2, lines 4-5, "said first output value" should be changed to --said first value--, and "said second output value" should be changed to --said second value--,

line 23, "said (1) and (2)" should be changed to --steps (1) and (2)--.

In claim 3, line 7, "its" should be changed to -- said bias adjustment circuit--.

In claim 4, line 7, "its" should be changed to -- said bias adjustment circuit--.

In claim 5, line 10, "its" should be changed to -- said bias adjustment circuit--.

In claim 6, lines 19-20, "said second and first capacitors" should be changed to --said second and first integrating capacitors--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Art Unit: 2816

As per claim 1, the limitation that “said first and second values being respective ones at respective times when first and second time intervals has elapsed after a given value having been step-inputted to said replica circuit” recited on lines 12-15 is not clear and confusing, i.e., it is unclear if the recitation means for each cycle of processing, a first voltage potential at the output of the replica circuit at a first predetermined time is taken and a second voltage potential at the output of the replica circuit at a second predetermined time is taken or means something else.

As per claim 2, the recitation that the control circuit causes an integral of the subtraction/integration circuit to be reset on lines 8-9 is unclear, i.e., it is unclear if the recitation means the subtraction/integration circuit is reset by the control circuit, the recitation that the control circuit repeats processing said given times on line 10 does not make sense, due to the problems discussed above, the limitations recited on lines 10-22 are unclear and confusing.

As per claim 3, the term “said bias current” recited on line 3 lacks clear antecedent basis, i.e., it is unclear if this is referring to the first or the second bias current, the terms “said successively summed value” recited on lines 4 and 7-8 lack clear antecedent basis, i.e., it is unclear if this is referring to the term “a value obtained by said successively summing” used on lines 17-18 of claim 1.

As per claim 4, the term “said bias current” recited on line 3 lacks clear antecedent basis, i.e., it is unclear if this is referring to the first or the second bias current, the terms “said successively summed value” recited on lines 4 and 7-8 lack clear antecedent basis, i.e., it is unclear if this is referring to the term “a value obtained by said successively summing” used on lines 17-18 of claim 1.

As per claims 5, the terms "said bias current" and "said successively summed value" recited on lines 3-7 and 11 lack clear antecedent basis for the same reasons noted in claim 3, "a given value" recited on line 12 lacks clear antecedent basis, i.e., it is unclear if this is referring to the given value recited on line 14-15 of claim 1.

As per claims 2-20, these claims are also rejected because of the indefiniteness of their independent claim 1.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No.

6,154,083 to Gaudet et al.

Gaudet discloses a semiconductor integrated circuit (Fig. 2) comprising:

an adjusted circuit 116 in which a first bias current IBIAS₂ flows, a slew rate of the adjusted circuit being dependent on the first bias current flow (since the rate of change of the adjusted circuit di/dt is affected by the first bias current flows);

Art Unit: 2816

a replica circuit 102 of the adjusted circuit 116 in which a second bias current IBIAS_1 flows, the limitation that the value of the second bias current being the same as the first bias current is met since the second bias current IBIAS_1 can be adjusted (column 4, line 39-40);

an evaluation circuit 108 (DLL LOGIC 108) configured to repeat processing (repeat every clock cycle), wherein the processing includes: resetting an output thereof (start the cycle), obtaining a difference between the first and second values (the signal from the output PAD of the replica circuit 102 is compared with the output signal from the DLL circuit) of an output of the replica circuit 102 at given times (specified by the clock signal), and the DLL circuit successively summing the differences (the signal from the output of the DLL circuit is the cumulation differences at a certain time);

a comparator circuit 110 (DAC) for comparing a value from the output of the DLL circuit with a reference value (the value supplies by the DAC 110 circuit); and

a bias adjustment circuit 112 (CURRENT MIRRORS) for changing the second bias current IBIAS_1 according to a comparison result of the comparator at every given times.

Allowable Subject Matter

4. Claims 2-20 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 2-8, 10-16 and 18-20 are allowable because the prior art of record fails to disclose or suggest a semiconductor integrated circuit which includes an evaluation circuit wherein the evaluation circuit includes a subtraction/integration circuit as recited in claim 2.

Art Unit: 2816

Claims 9 and 17 are allowable because the prior art of record fails to disclose or suggest a semiconductor integrated circuit which includes an adjusted circuit wherein the adjusted circuit includes an operational amplifier circuit as recited in claim 9.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. 5,107,224 to Meyer discloses a semiconductor integrated circuit (Fig. 1) which includes an adjusted circuit 15c, a replica circuit 99, an evaluation circuit 17, a comparator circuit 19 and a bias adjustment circuit 19a.

US Patent No. 5,831,562 to Van Auken et al discloses a semiconductor integrated circuit (Fig. 1B) which can be used for implementing an adjusted circuit.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday - Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Art Unit: 2816

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

A handwritten signature in black ink, appearing to read 'Minh Nguyen', with a horizontal line underneath.

Minh Nguyen
Examiner
Art Unit 2816

March 20, 2002